WHAT IS CLAIMED IS:

1. A heterojunction field effect transistor, comprising:

a semiconductor layer forming substrate formed with a plurality of semiconductor layers on a semi-insulative substrate,

a gate electrode formed on said semiconductor layer forming substrate,

N-type source area and drain area formed by carrying out ion implantation to form N-type semiconductor on predetermined areas in said semiconductor layer forming substrate at both sides of said gate electrode, and by carrying out annealing process for activating the ion implanted areas,

an active layer including a predetermined semiconductor layer in said plurality of semiconductor layers between said source area and said drain area, and

an N-type carrier supply layer for supplying electron to said active layer formed of the upper or both of the upper and lower said semiconductor layers of said active layer between said source area and said drain area,

wherein at least one of the semiconductor layers to be said N-type carrier supply layer is doped with Selenium (Se) or Tellurium (Te).

2. The heterojunction field effect transistor according to claim 1, wherein the semiconductor layer that serves as said

active layer, is an InGaAs layer, and the semiconductor layer that serves as said N-type carrier supply layer is an AlGaAs layer.

3. The heterojunction field effect transistor according to claim 1, wherein the semiconductor layer that serves as said active layer is an InGaAs layer, the semiconductor layer that serves as said N-type carrier supply layer is an InAlAs layer.

4. The heterojunction field effect transistor according to claim 1, wherein the semiconductor layer that serves as said active layer is a GaAs layer, and the semiconductor layer that serves as said N-type carrier supply layer is an AlGaAs layer.

5. A heterojunction field effect transistor, comprising:

a semiconductor layer forming substrate formed with a plurality of semiconductor layers on a semi-insulative substrate,

a gate electrode formed on said semiconductor layer forming substrate,

N-type source area and drain area formed by carrying out ion implantation to form N-type semiconductors on predetermined areas in said semiconductor layer forming substrate at both sides of said gate electrode and by carrying out annealing process for activating the ion implanted areas, and

an N-type active layer formed of a predetermined semiconductor layer in said plurality of semiconductor layers

between said source area and said drain area,

wherein the semiconductor layer to be said N-type active layer is doped with Selenium(Se) or Tellurium(Te).

6. The heterojunction field effect transistor according to claim 5, wherein the semiconductor layer that serves as said N-type active layer is either one of InGaAs layer, GaAs layer and InP layer.

7. A manufacturing method of a heterojunction field effect transistor, comprising the steps of:

forming a semiconductor layer forming substrate having a plurality of semiconductor layers including at least a semiconductor layer, which serves as an active layer, and a semiconductor layer at the upper side or at the both upper and lower sides of said active layer, which serves as an N-type carrier supply layer for supplying electron to said active layer, on a semi-insulative substrate,

forming a gate electrode on said semiconductor layer forming substrate, and

forming N-type source area and drain area by carrying out ion implantation for forming N-type semiconductors in predetermined areas of said semiconductor layer forming substrate at the both sides of said gate electrode and by carrying out annealing process for activating the ion implanted areas,

wherein, when forming said semiconductor layer forming

substrate, at least one semiconductor layer to be said N-type carrier supply layer is doped with Selenium (Se) or Tellurium (Te).

8. The manufacturing method of a heterojunction field effect transistor according to claim 7, wherein, when forming said semiconductor layer forming substrate, an InGaAs layer is formed as the semiconductor layer, which serves as said active layer, and an AlGaAs layer is formed as the semiconductor layer, which serves as said N-type carrier supply layer.

9. The manufacturing method of a heterojunction field effect transistor according to claim 7, wherein, when forming said semiconductor layer forming substrate, an InGaAs layer is formed as the semiconductor layer, which serves as said active layer, and an InAlAs layer is formed as the semiconductor layer, which serves as said N-type carrier supply layer.

10. The manufacturing method of a heterojunction field effect transistor according to claim 7, wherein, when forming said semiconductor layer forming substrate, a GaAs layer is formed as the semiconductor layer, which serves as said active layer, and an AlGaAs layer is formed as the semiconductor layer, which serves as said N-type carrier supply layer.

11. A manufacturing method of a heterojunction field effect transistor, comprising the steps of:

forming a semiconductor layer forming substrate having a plurality of semiconductor layers including at least a

semiconductor layer, which serves as an N-type active layer, on a semi-insulative substrate,

forming a gate electrode on said semiconductor layer forming substrate, and

forming N-type source area and drain area by carrying out ion implantation for forming N-type semiconductors in predetermined areas of said semiconductor layer forming substrate at the both sides of said gate electrode and by carrying out annealing process for activating the ion implanted areas,

wherein, when forming said semiconductor layer forming substrate, said semiconductor layer to be said N-type active layer is doped with Selenium(Se) or Tellurium(Te).

12. The manufacturing method of a heterojunction field effect transistor according to claim 11, wherein, when forming said semiconductor layer forming substrate, any one of InGaAs layer, GaAs layer and InP layer is formed as the semiconductor layer, which serves as said N-type active layer.

13. The manufacturing method of a heterojunction field effect transistor according to claim 7, wherein annealing process carried out for forming said N-type source area and drain area is carried out in a manner of lamp annealing.

14. The manufacturing method of a heterojunction field effect transistor according to claim 11, wherein annealing process carried out for forming said N-type source area and

drain area is carried out in a manner of lamp annealing.